

Advanced Computer Architecture

Lecture 20

Tiled Chip Multicore Processors



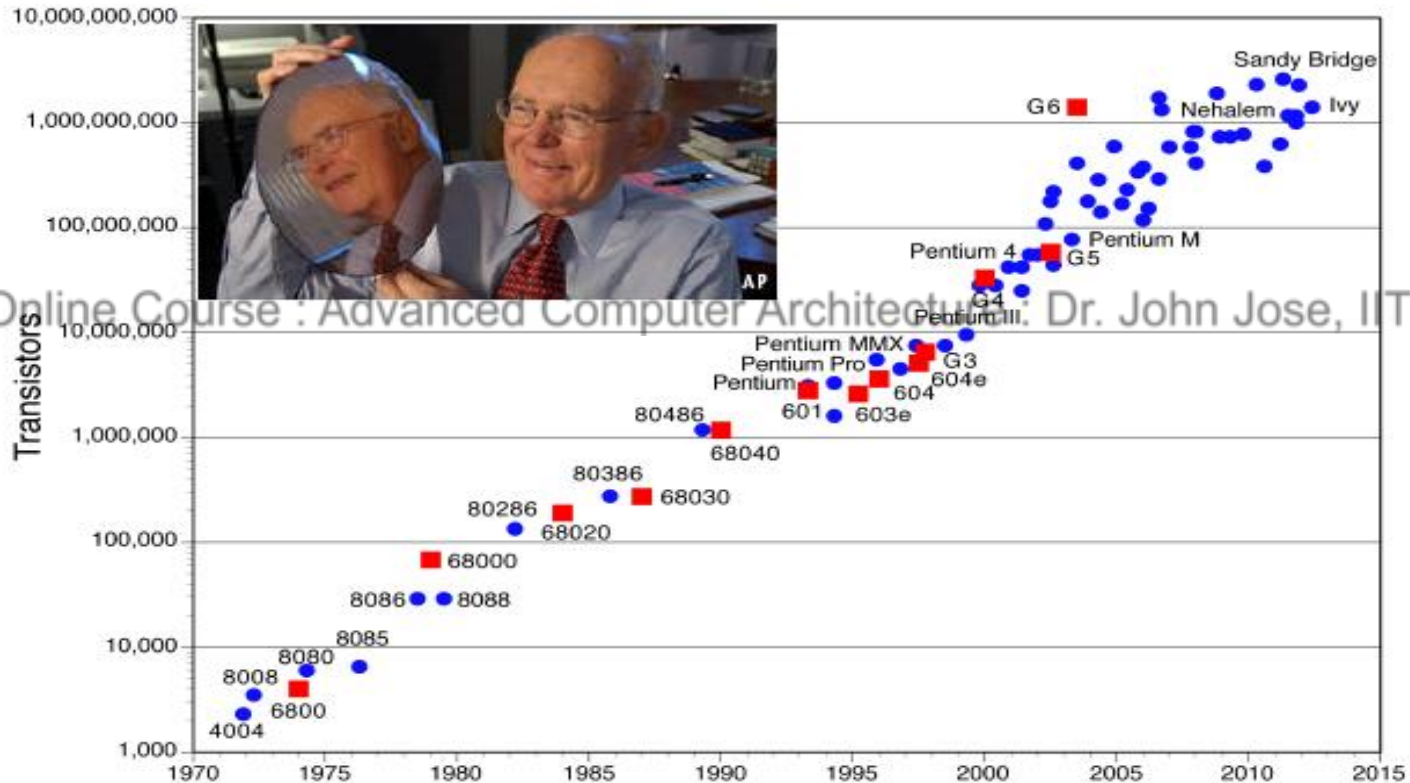
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Dr. John Jose

Assistant Professor

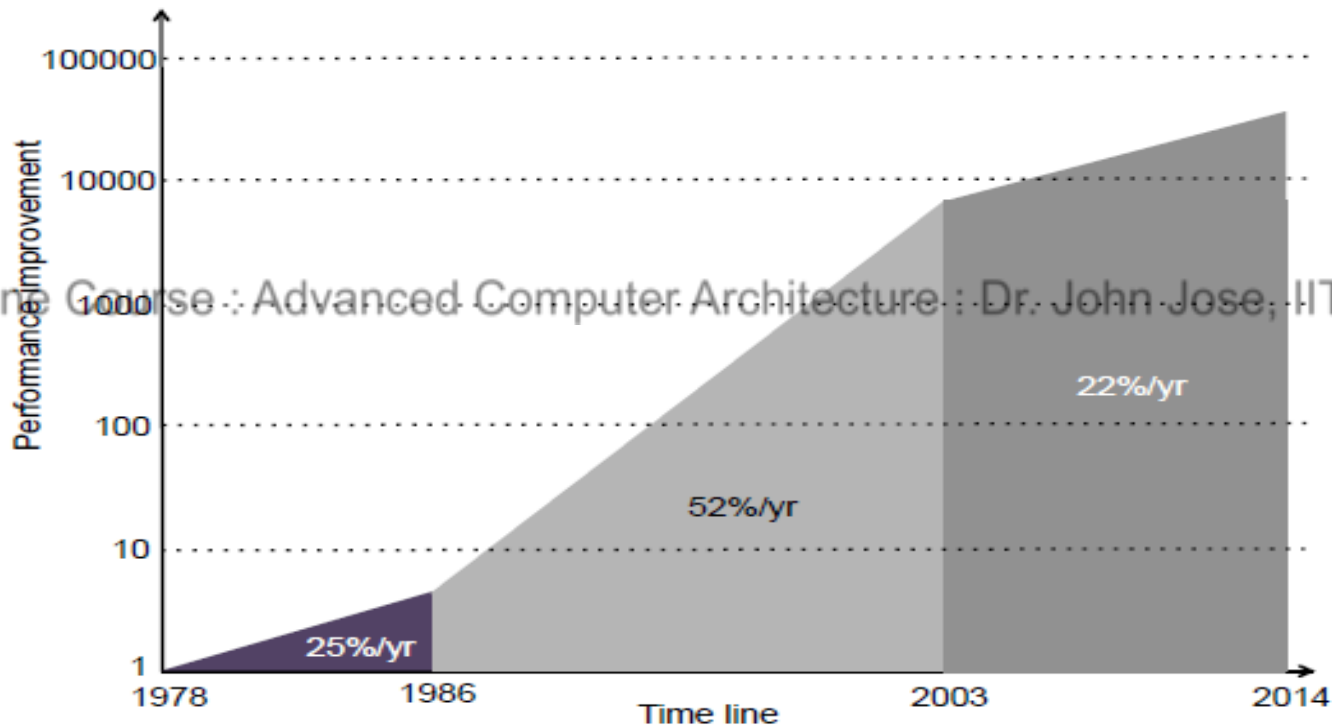
**Department of Computer Science & Engineering
Indian Institute of Technology Guwahati, Assam.**

Impact of VLSI in processor trends



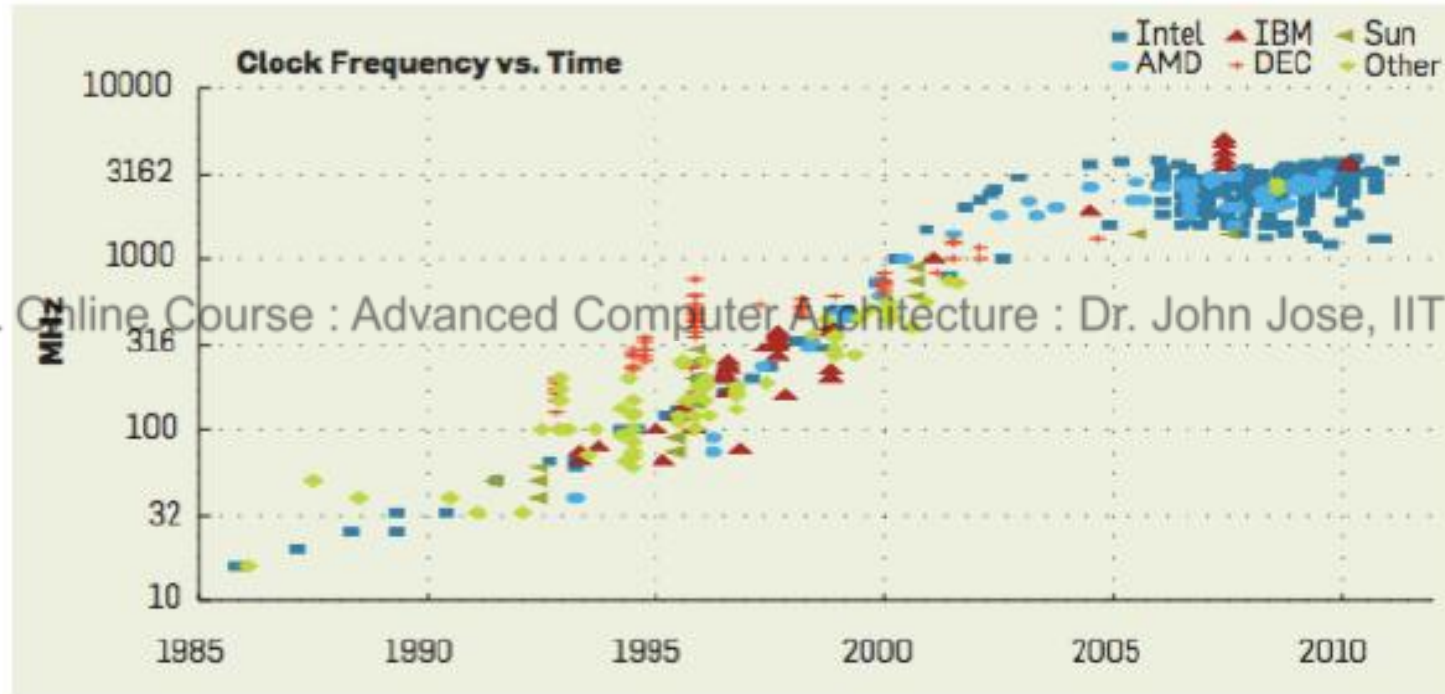
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Processors Performance

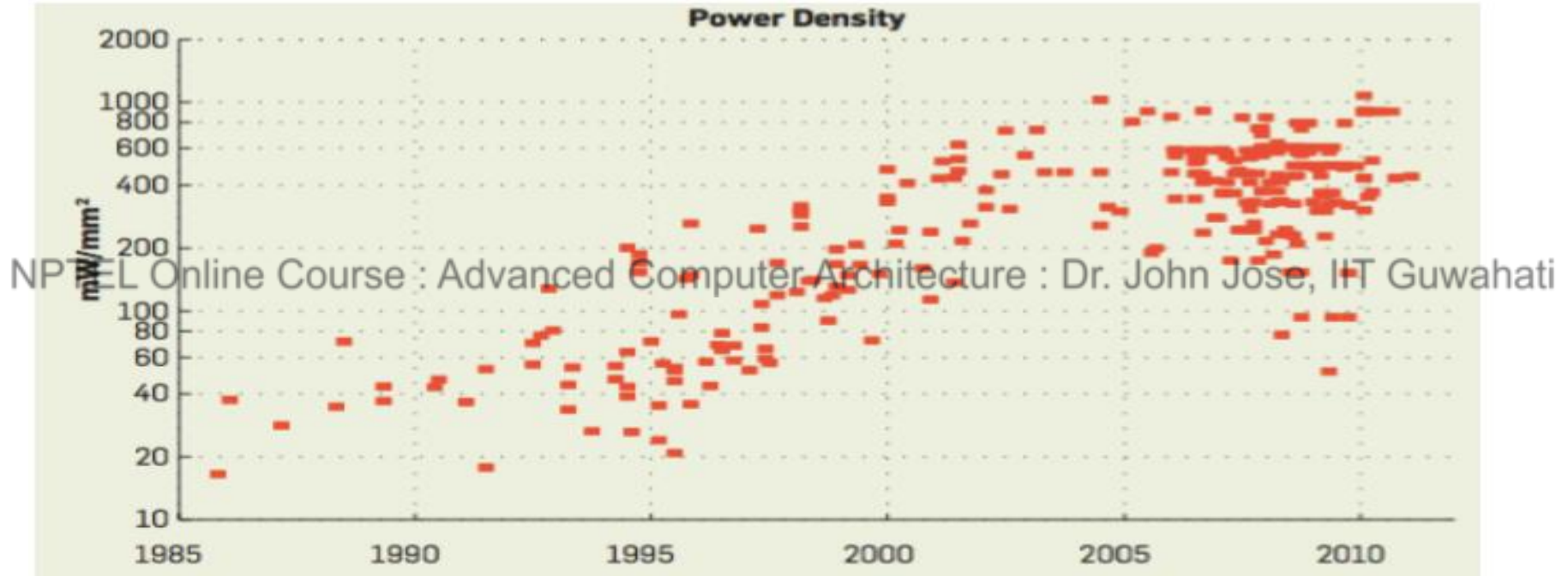


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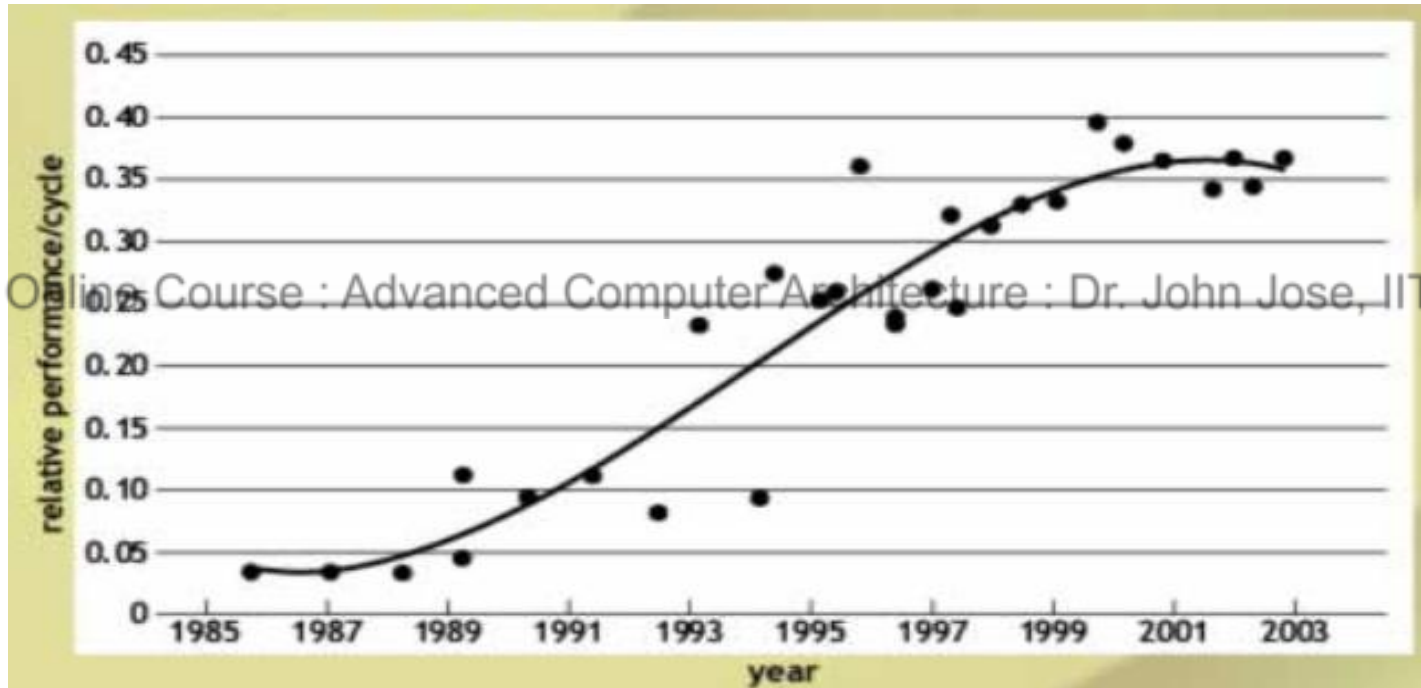
Frequency Wall



Power Wall

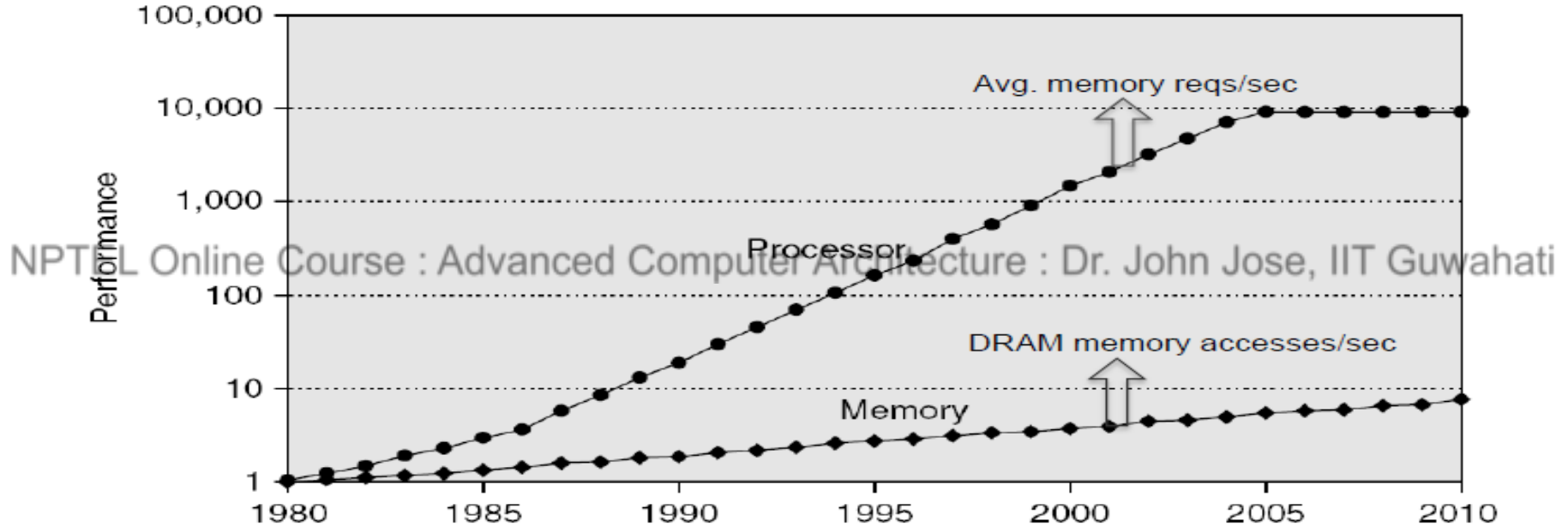


ILP Wall



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Memory Wall

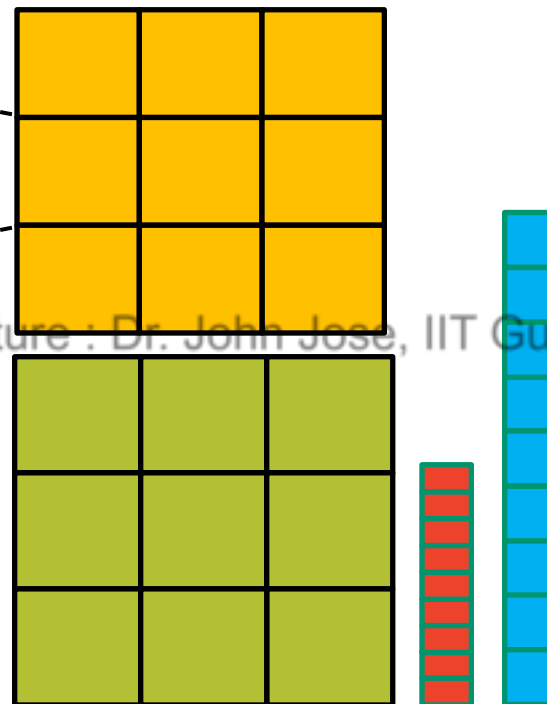


Paradigm Shift to Multicore

2004 SoC : 90 nm



2017 SoC : 10 nm



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Multiple slower processors vs single fast powerful processor

Paradigm Shift to Multicore



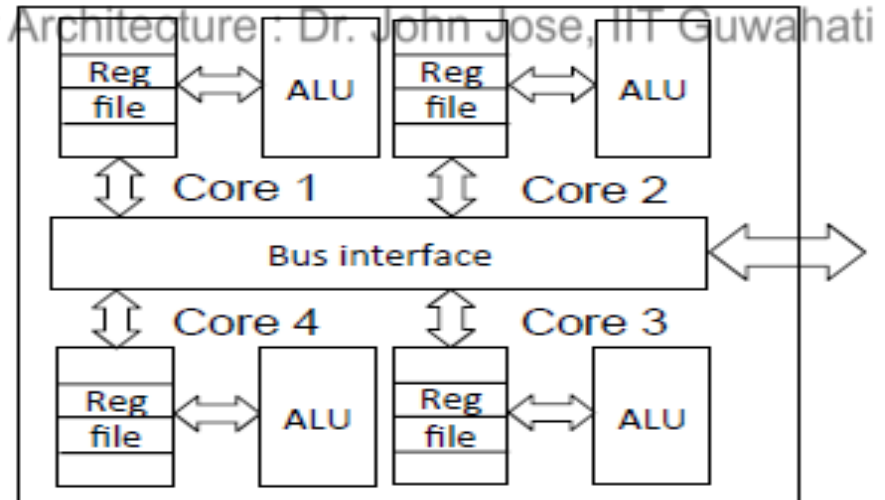
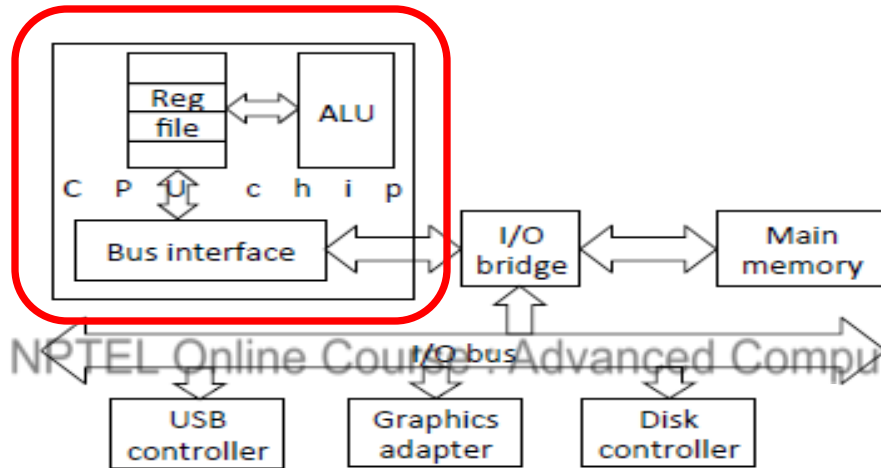
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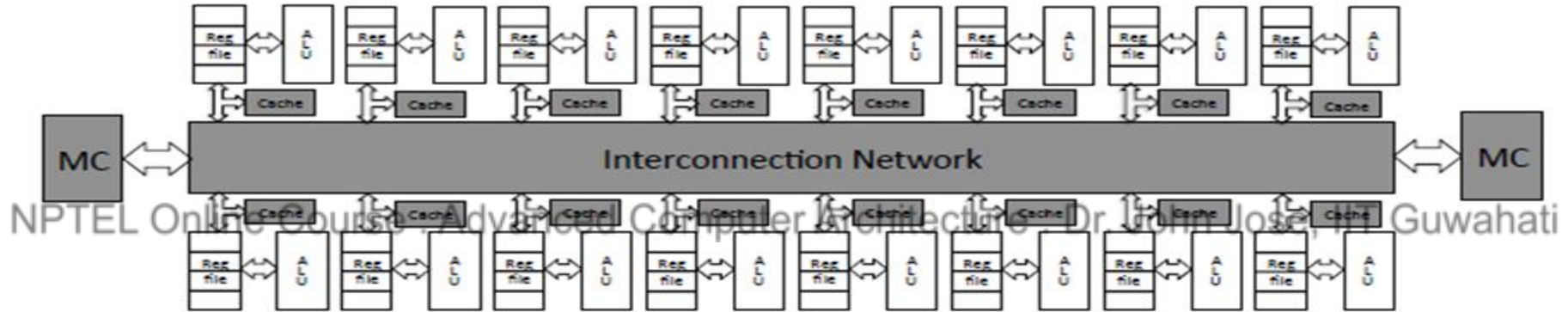
Multiple slower processors is better than single fast powerful processor

What is Multicore ?



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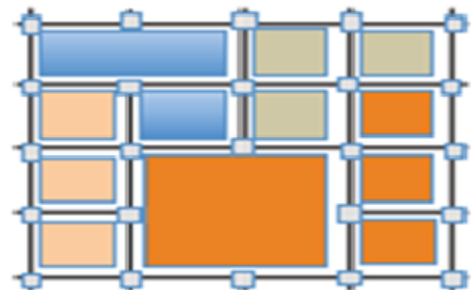
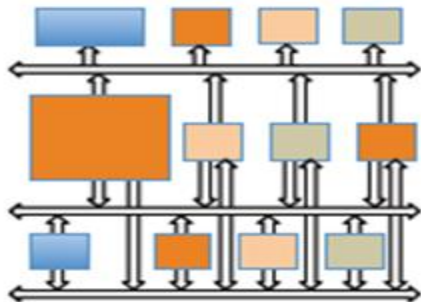
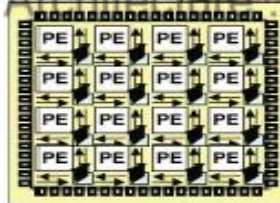
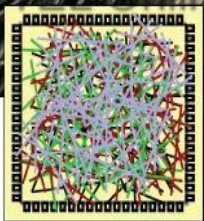
What is Multicore ?



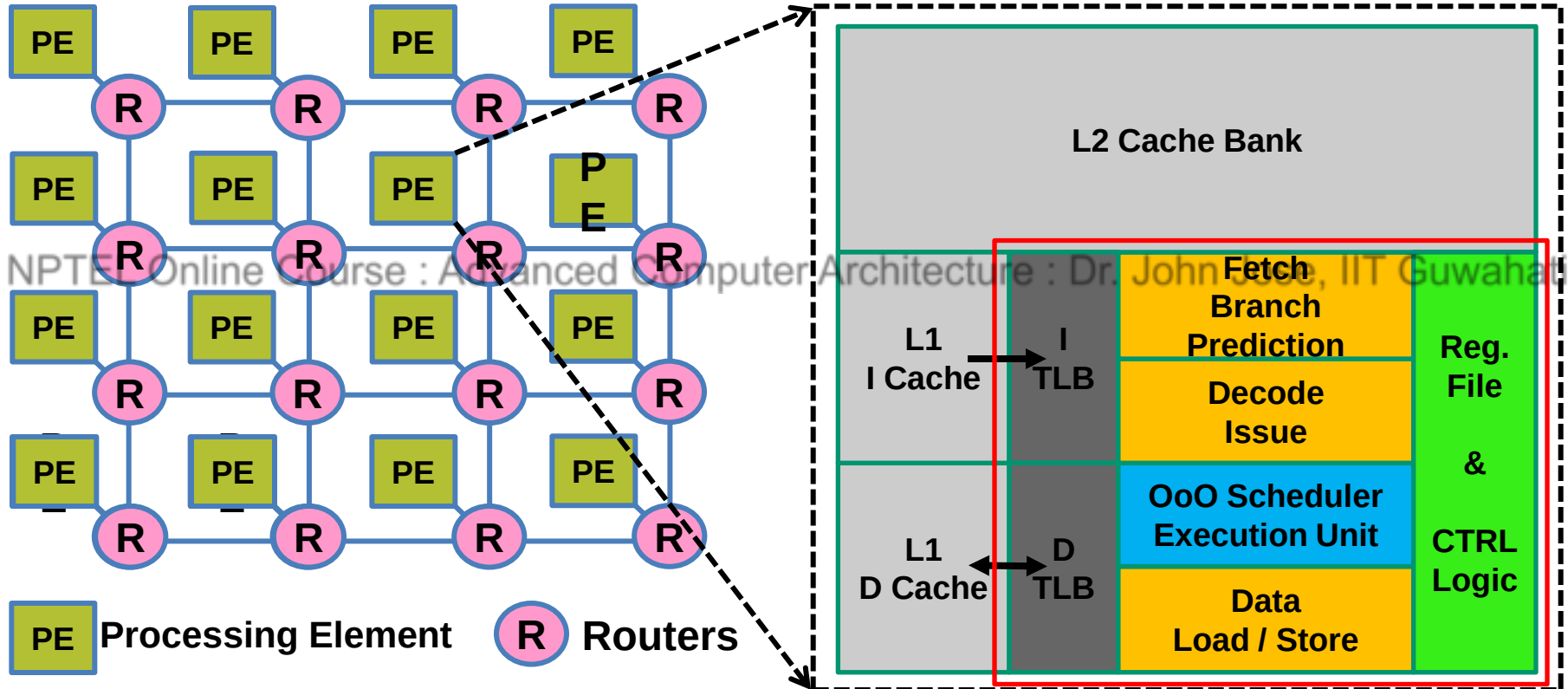
❖ How these cores communicate ?

❖ What is the best interconnection mechanism ?

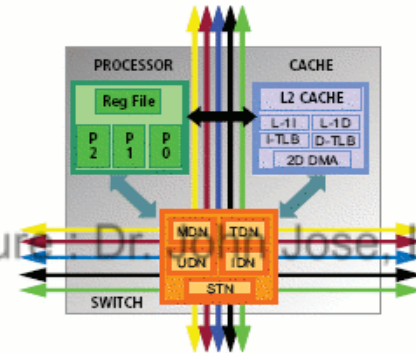
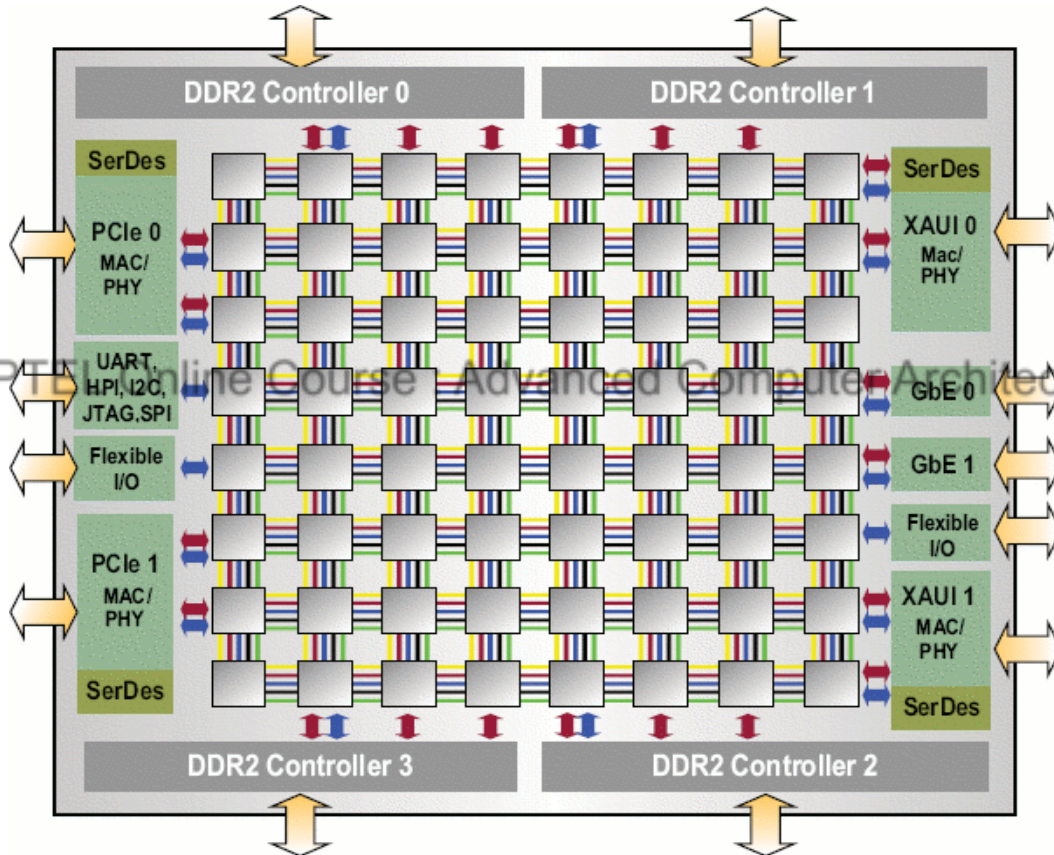
The Paradigm Shift



Tiled Chip Many-Core Processor (TCMP)

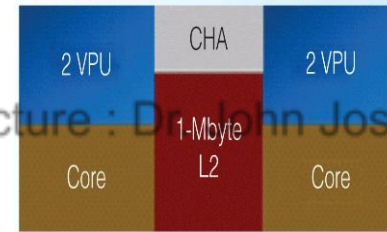
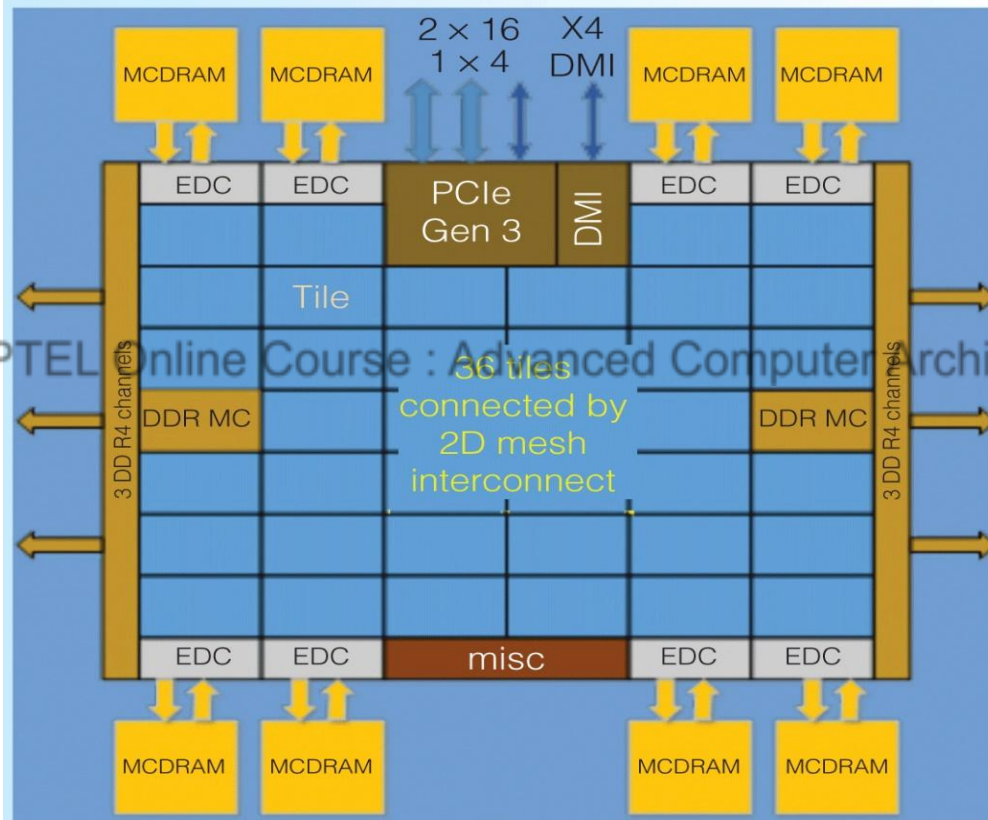


State-of-the-Art Architectures



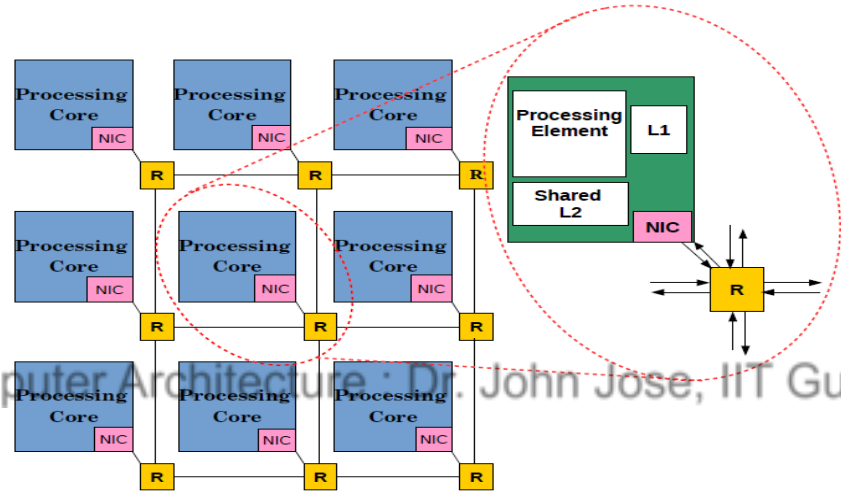
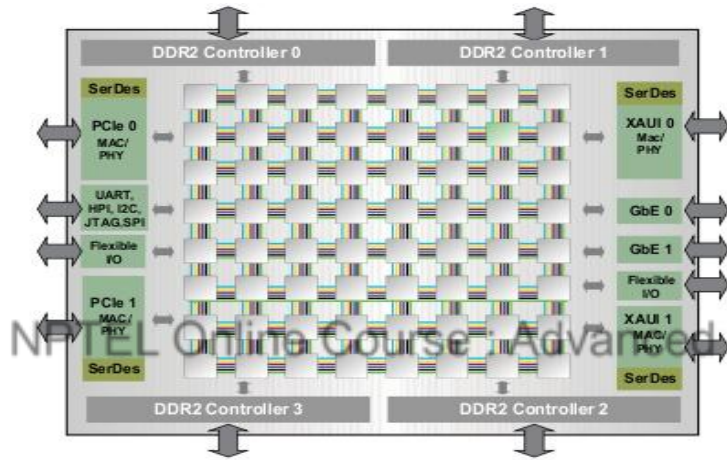
Tilera64

State-of-the-Art Architectures



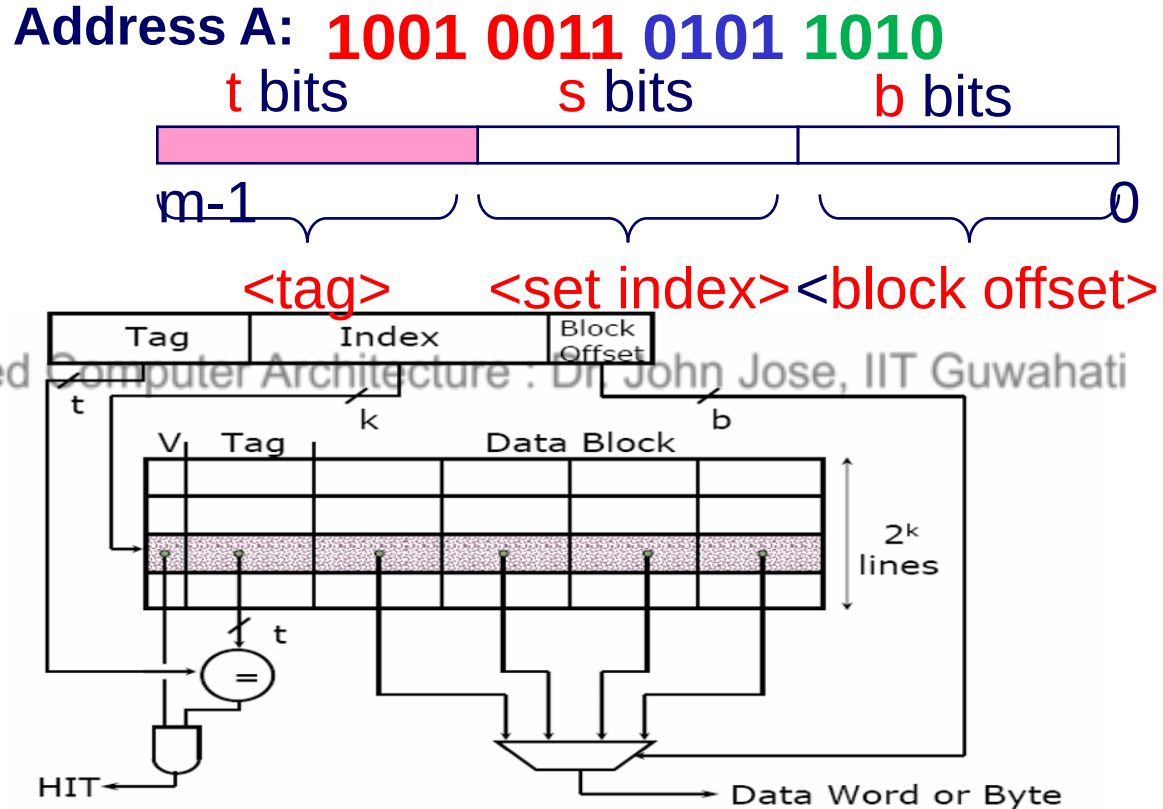
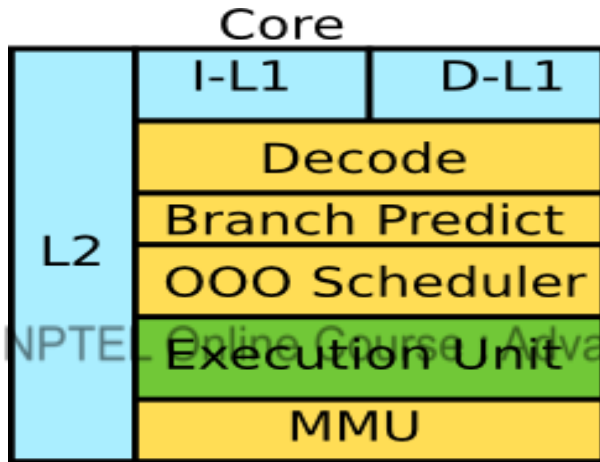
Intel KNL

Routers and Tiles

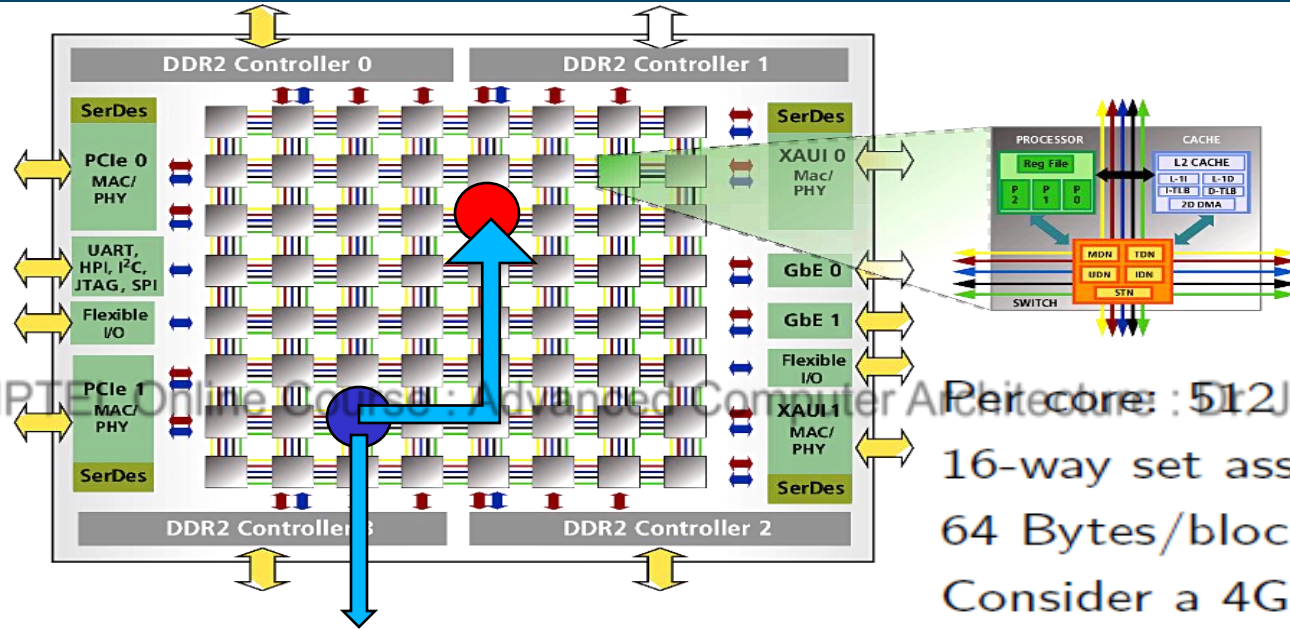


- ❖ East, West, North and South neighbors
- ❖ Packets are divided into flow control units called flits
- ❖ L1 and L2 cache misses create NoC traffic packets

What is the role of on-chip cache ?



On-Chip Cache Address Mapping



Per core: 512 KB Jose, IIT Guwahati

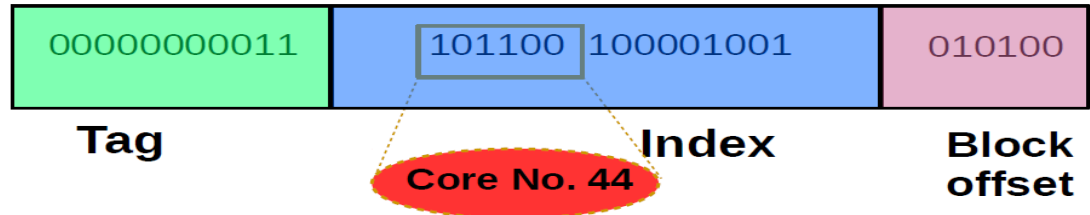
16-way set associative mapping

64 Bytes/block

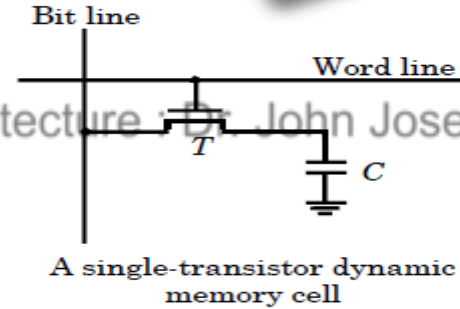
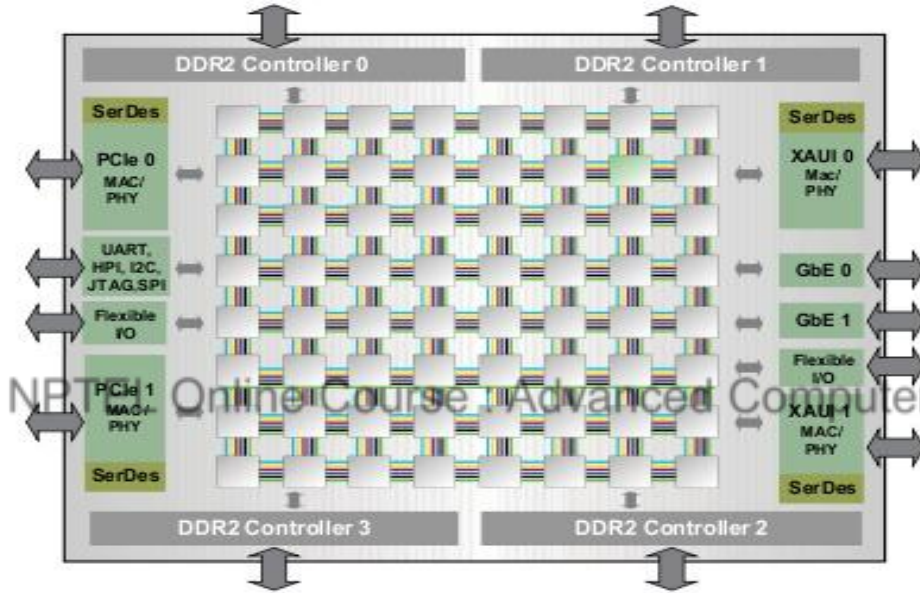
Consider a 4GB RAM (2^{32} bits)

Hex Address : 0x764254

11 bits	15 bits	6 bits
Tag	Index	Block offset



What is the role of memory controllers?



**THANK
YOU!**

FOR

YOUR

PRESENCE

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